

02/07/00



02-09-00

A

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.: 2933SE-90

Inventors: Toshio NAKAKUKI of 1069-5, Honden, Hozumi-cho, Motosu-gun, Gifu-ken 501-0236 Japan
Tomomichi NAKAI of 2-18, Sanbongi, Ogaki-shi, Gifu-ken 503-0813 Japan

Express Mail Label No.: IB914059212

Title: "SOLID-STATE IMAGING APPARATUS WITH EXPOSURE CONTROL"

Assistant Commissioner for Patents

Box Patent Application

Washington, DC 20231

35713 U.S. PTO
09/499229
02/07/00

Enclosed for filing with the above-identified utility patent application, please find the following:

1. [X] Specification (Total Pages of Text, including Abstract and Claims: 17)
2. [X] Drawing(s) (35 USC 113) (Total Sheets: 3) [X] FORMAL [] INFORMAL
3. [X] Oath or Declaration (Total Pages: 3) [X] Signed [] Unsigned
4. [X] Assignment Papers (cover sheet & document(s))
5. [X] Return Postcard (MPEP 503) (should be specifically itemized)
6. [X] A check in the amount of \$690.00 is enclosed.

FEE CALCULATION:

	(COL. 1) NO. FILED			(COL. 2*) NO. EXTRA		SMALL ENTITY			LARGE ENTITY	
						RATE	FEE		RATE	FEE
BASIC FEE:							\$345.00	OR		\$690.00
TOTAL CLAIMS:	11	-	20		0	X \$9 =		OR	X \$18 =	\$0.00
INDEP. CLAIMS:	2	-	3		0	X \$39 =		OR	X \$78 =	\$0.00
MULTIPLE DEPENDENT CLAIMS						+ \$130 =		OR	+\$260 =	\$0.00
*IF THE DIFFERENCE IN COL. 2 IS LESS THAN ZERO, ENTER "0" IN COL. 2.						TOTAL:				\$690.00

OTHER INFORMATION:

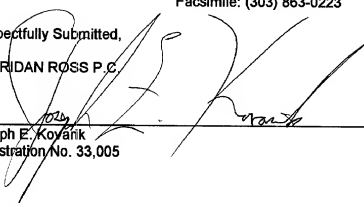
1. [X] The Commissioner is hereby authorized to debit any underpayments or credit any overpayment to Deposit Account No. 19-1970.
2. [X] The Commissioner is hereby authorized to charge all required fees for extensions of time under \$1.17 to Deposit Account No. 19-1970.
3. [X] Foreign Priority benefits are claimed under 35 USC §119 of Japanese Patent Application Serial No. 11-030377 filed February 8, 1999.

4. Correspondence Address:

Joseph E. Kovarik, Esq.
SHERIDAN ROSS P.C.
1560 Broadway, Suite 1200
Denver, Colorado 80202-5141
Telephone: (303) 863-9700
Facsimile: (303) 863-0223

Respectfully Submitted,

SHERIDAN ROSS P.C.



Joseph E. Kovarik
Registration No. 33,005

Date: 2/7/00

SOLID-STATE IMAGING APPARATUS WITH EXPOSURE CONTROL

BACKGROUND OF THE INVENTION

The present invention relates to a solid-state imaging apparatus, and more particularly, to a solid-state imaging apparatus having an exposure control function.

Fig. 1 is a schematic block diagram of a conventional solid-state imaging apparatus 100 and Fig. 2 is a timing waveform chart which describes the operation of the solid-state imaging apparatus 100. The solid-state imaging apparatus 100 includes a CCD image sensor 1, a driver 2, a timing control circuit 3, an integrating circuit 4, a decision circuit 5, an up/down counter 6 and a latch circuit 7.

The CCD image sensor 1 has a plurality of light receiving pixels, a plurality of vertical shift registers and a horizontal shift register. The light receiving pixels are arranged on a light receiving surface in lines at predetermined intervals, and generate and store information charges corresponding to an object image. The vertical shift registers are arranged in columns corresponding to the lines of light receiving pixels, and sequentially transfer the information charges stored in each of the light receiving pixels in the vertical direction. The horizontal shift register is arranged on the output side of the vertical shift registers, receives the information charges output from the vertical shift registers, and outputs the charges in a unit of one line. In this manner, an image signal Y with a changing a voltage value in accordance with the information charges stored in the light receiving pixels is output.

The driver 2 supplies each shift register of the CCD 1 with a multi-phase transfer clock in response to a vertical synchronous signal VD and a horizontal synchronous signal HD from the timing control circuit 3. The driver 2 produces a frame transfer clock ϕF in response to the vertical synchronous signal VD and supplies the vertical shift register with the frame transfer clock ϕF . The information charges stored in the light receiving pixels are transferred to the vertical shift registers every vertical scanning period in accordance with the frame transfer clock ϕF . The driver 2 produces a storage transfer clock ϕS and a horizontal transfer clock ϕH in response to the horizontal synchronous signal HD. The vertical shift registers transfer the information charges to the horizontal shift register in accordance with the storage transfer clock ϕS , and the horizontal shift register outputs the information charges in a unit of one line in accordance with the horizontal transfer clock ϕH . The driver 2 produces a drain clock ϕD in response to a shutter timing signal ST from the timing control circuit 3. The drain clock ϕD is supplied to an unnecessary charge drain region of the CCD 1 and the information charges stored in the light receiving pixels are drained to this drain region. A period L from the end of the drain clock ϕD to the start of the frame transfer clock ϕF is defined as the information charges storage period, or the so-called exposure time.

The timing control circuit 3 frequency-divides a reference clock CK having a predetermined period and produces the vertical synchronous signal VD which determines the vertical scan timing of the CCD 1 and the horizontal synchronous signal HD which determines the horizontal scan timing. For example, in conformity with the NTSC (National Television System Committee) standard, the horizontal

synchronous signal HD is produced by setting the reference clock CK to 14.32 MHz and frequency-dividing it into 910 parts. The vertical synchronous signal VD is produced by further frequency-dividing the horizontal synchronous signal HD into 252.5 parts.

The integrating circuit 4 integrates the image signal Y output from the CCD 1 in units of a vertical scan periods and produces integration value information IY which is proportional to the average level of the image signal Y. The integrating circuit 4 is reset with the vertical synchronous signal VD.

The decision circuit 5 receives the integration value information IY from the integrating circuit 4, compares the integration value information IY with upper and lower limits which correspond to an appropriate vertical scanning period exposure range, and activates an exposure suppression signal CL or an exposure acceleration signal OP based on the comparison results. If the integration value information IY exceeds the upper limit, the exposure suppression signal CL is activated, and if the integration value information IY is below the lower limit, the exposure acceleration signal OP is activated.

The up/down counter 6 performs an up count operation when the exposure suppression signal CL is activated and performs a down count operation when the exposure acceleration signal OP is activated. A counted value of the up/down counter 6 corresponds to a horizontal scan line number and the timing of the shutter timing signal ST is determined in accordance with the horizontal scan line number.

The latch circuit 7 latches the counted value of the up/down counter 6 every vertical scan period in accordance with the vertical synchronous signal VD and supplies the timing control circuit 3 with the counted value as exposure information D. There are plurality of horizontal scan periods for each vertical scan period. The timing control circuit 3 activates the shutter timing signal ST based on the exposure information D when the horizontal scan period, which corresponds to the counted value of the up/down counter 6, has elapsed from the start of the vertical scanning period. The exposure time L is extended or shortened every vertical scan period in a unit of one horizontal scan period by performing the up count or down count operation in accordance with the integration value information IY of the image signal Y.

If the level of an image signal is within the range of appropriate exposure, as determined by the decision circuit 5, the exposure time L is not extended or shortened, and system control circuit does not respond to a slight change of luminance of the sensed object. Therefore, a change in the object luminance appears as a change in the image signal. Accordingly, if the brightness of illumination is not stable, the brightness of the illumination appears on a reproduction screen. Further, if a light source which emits light periodically is used, the emission period and imaging period of the light source may substantially coincide. In this case, if a jitter is contained in the emission period of the light source, the average level of the image signal varies due to the jitter. The fluctuation of the average level of such image signal causes a flicker having a long period on the reproduction screen.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a solid-state imaging apparatus with accurate exposure timing. A solid-state imaging apparatus, comprising:

In one aspect of the present invention, a solid-state imaging apparatus is provided. The imaging apparatus includes a solid-state image sensor for accumulating information charges corresponding to an image of an object and generating an image signal in response to the information charges. The image sensor includes a driver, connected to the image sensor, for driving the image sensor in accordance with a timing signal so that the information charges are accumulated in a predetermined exposure period, and for outputting the image signal from the image sensor. A first exposure information generating circuit determines whether a level of the image signal output from the image sensor is within a predetermined range and produces first exposure information based on the determination results. A second exposure information generating circuit calculates second exposure information using the image signal output from the image sensor. A selection circuit is connected to the first and second exposure information generating circuit s to select the first exposure information when the level of the image signal is outside of the predetermined range and select the second exposure information when the level of the image signal is within the predetermined range. A timing control circuit is connected to the driver to receive the exposure information selected by the selection circuit and generates the timing signal therefrom. The timing signal defines the predetermined exposure period.

In another aspect of the present invention, a method for controlling an exposure period of a solid-state imaging apparatus is provided. The imaging apparatus includes a

solid-state image sensor which accumulates information charges corresponding to an object image and generates an image signal in response to the information charges. First, the solid-state image sensor is driven in accordance with a timing signal so that the information charges are accumulated within the exposure period and the image signal is output. Then, whether a level of the image signal output from the solid-state image sensor is within a predetermined range is determined and first exposure information is generated based on the determination results. Second exposure information is calculated using the image signal output from the solid-state image sensor. Then, the first exposure information is selected when the level of the image signal is outside of the predetermined range and the second exposure information is selected when the level of the image signal is within the predetermined range. The timing signal for setting the exposure period is generated in accordance with the selected exposure information.

Other aspects and advantages of the invention will become apparent from the following description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention, together with objects and advantages thereof, may best be understood by reference to the following description of the presently preferred embodiments together with the accompanying drawings in which:

Fig. 1 is a schematic block diagram of a conventional solid-state imaging apparatus;

Fig. 2 is a timing chart which describes the operation of the solid-state imaging apparatus of Fig. 1;

Fig. 3 is a schematic block diagram of a solid-state imaging apparatus according to one embodiment of the present invention; and

Fig. 4 is a graph showing the relationship between an exposure time and the integration value of an image signal.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the drawings, like numerals are used for like elements throughout.

Fig. 3 is a schematic block diagram of a solid-state imaging apparatus 200 according to one embodiment of the present invention, and Fig. 4 is a graph showing the relationship between the exposure time of a CCD image sensor 1 and an integration value of an image generated by the apparatus 200.

The solid-state imaging apparatus 200 comprises the CCD image sensor 1, the driver 2, the timing control circuit 3, an integrating circuit 11, an exposure decision circuit 12, an up/down counter 13, a timing calculation circuit 14, a selection circuit 15 and a latch circuit 16. The driver 2 pulse-drives the CCD image sensor 1 in accordance with various signals from the timing control circuit 3 and an image signal Y is output from the CCD image sensor 1.

In one embodiment of the present invention, first exposure information D1 for controlling a length of the exposure time L of the CCD image sensor 1 in a predetermined step and second exposure information D2 for specifying the optimum exposure time length L are selectively supplied to the timing control circuit 3. More specifically, if the exposure state of the CCD image sensor 1 is out of the predetermined range, the first exposure information D1 is

supplied to the timing control circuit 3. After the exposure state of the CCD image sensor 1 has become appropriate (i.e., within the predetermined range) by either extending or shortening the exposure time L based on the first exposure information D1, the second exposure information D2 is supplied to the timing control circuit 3.

The integrating circuit 11 integrates an image signal Y output from the CCD image sensor 1 each vertical scan period and generates integration value information IY which proportional to the average level of the image signal Y.

The exposure decision circuit 12 receives the integration information IY from the integrating circuit 11, compares the integration value information IY with upper and lower limits of the predetermined exposure range, and activates any one of an exposure suppression signal CL, an exposure acceleration signal OP and an exposure fixed signal HLD based on the compare result. Specifically, if the integration value information IY exceeds the upper limit, the exposure suppression signal CL is activated. If the integration value information IY is below the lower limit, the exposure acceleration signal OP is activated. If the integration value information IY is between the upper and lower limits, the exposure fixed signal HLD is activated. The exposure decision circuit 12 is reset with a vertical synchronous signal VD.

The up/down counter 13 performs an up count operation in response to the exposure suppression signal CL and performs a down count operation in response to the exposure acceleration signal OP. The counter value of the up/down counter 13 is supplied to the selection circuit 15 as the first exposure information D1. The first exposure

information D1 corresponds to a horizontal scan line number which determines the activation timing of a shutter timing signal ST output from the timing control circuit 3. The first exposure information D1 (counter value) is updated every vertical scan period and is incremented and decremented by one during each vertical scan period. By the increment and decrement of the counter value, the exposure time L of the CCD image sensor 1 is extended or shortened in units of one horizontal scan period. The exposure decision circuit 12 and the up/down counter 13 form a first exposure information generating circuit .

The timing calculation circuit 14 holds exposure information D which is output from the latch circuit 16 and corresponds to the current exposure time L of the CCD image sensor 1 and calculates the second exposure information D2 using the ratio of the integration value information IY to the exposure information D and the optimum value R0 which corresponds to the optimum exposure state. That is, the second exposure information D2 is calculated in accordance with the following expression:

$$D2 = R0 \times D/IY$$

The optimum value R0 is a predetermined value. The second exposure information D2 is calculated when the integration value information IY and the exposure information D are determined, and the activation timing of the shutter timing signal ST by the timing control circuit 3 is determined based on the second exposure information D2. The timing calculation circuit 14 serves as a second exposure information generating circuit .

The selection circuit 15 is connected to the up/down

counter 13 and the timing calculation circuit 14 and selects the first exposure information D1 or the second exposure information D2 in response to the exposure fixed signal HLD. That is, if the exposed state of the CCD1 is outside of the predetermined, appropriate range and thus, the exposure fixed signal HLD is not activated, the first exposure information D1 is selected. In response, the exposure time L is extended or shortened every vertical scan period in units of one horizontal scan period based on the first exposure information D1. If the exposure state of the CCD image sensor 1 is within the appropriate range and the exposure fixed signal HLD is activated, the second exposure information D2 is selected. In this case, the exposure time L is determined based on the second exposure information D2.

The latch circuit 16 latches the exposure information selected by the selection circuit 15 in accordance with a vertical synchronous signal VD and supplies the timing control circuit 3 and the timing calculation circuit 14 with the exposure information D.

Next, the operation of the solid-state imaging apparatus 200 is described. Until the exposure state is included within the appropriate range, the exposure time L is extended or shortened based on the first exposure information D1 in the same manner as a conventional example. If the exposure state is included within the appropriate range, the exposure time L is determined in unit of one step based on the second exposure information D2.

For example, as shown in Fig. 4, at point A of the graph which corresponds to the exposure time L (L1), if the corresponding integration value information IY (i1) does not reach the appropriate lower limit RL, the first exposure

information D1 is selected and the exposure time L is extended by one horizontal scan period. The extension of the exposure time L is repeated until the integration value information IY exceeds the appropriate lower limit RL. If the integration value information IY exceeds the lower limit RL, the first exposure information D1 is switched to the second exposure information D2. Then, the exposure time L2 which corresponds to the intermediate optimum value i2 between the upper limit RH and the lower limit RL is determined based on the second exposure information D2. Thus, the exposure state converges at point B of the graph of Fig. 4.

As described above, according to one embodiment of the present invention, the exposure time control of the CCD image sensor 1 is always performed and the exposure state converges at the optimum value within the appropriate range. At this time, since the exposure time is adjusted every horizontal scan period until the exposure state is within the appropriate range, a sudden change of an image signal level due to a sudden change of the exposure time is prevented. Further, even after the exposure state is within the appropriate range, exposure control is performed. Thus, the average level of the image signal Y becomes stable without being affected by a change in the brightness of illumination and the emission period.

It should be apparent to those skilled in the art that the present invention may be embodied in many other specific forms without departing from the spirit or scope of the invention. Therefore, the present examples and embodiments are to be considered as illustrative and not restrictive and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalence

of the appended claims.

10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

WHAT IS CLAIMED IS:

1. A solid-state imaging apparatus, comprising:
a solid-state image sensor for accumulating information
charges corresponding to an image of an object and
generating an image signal in response to the information
charges;

a driver, connected to the image sensor, for driving
the image sensor in accordance with a timing signal so that
the information charges are accumulated in a predetermined
exposure period, and for outputting the image signal from
the image sensor;

a first exposure information generating circuit for
determining whether a level of the image signal output from
the image sensor is within a predetermined range and
producing first exposure information based on the
determination results;

a second exposure information generating circuit for
calculating second exposure information using the image
signal output from the image sensor;

a selection circuit, connected to the first and second
exposure information generating circuit s, for selecting the
first exposure information when the level of the image
signal is outside of the predetermined range and selecting
the second exposure information when the level of the image
signal is within the predetermined range; and

a timing control circuit, connected to the driver, for
receiving the exposure information selected by the selection
circuit and generating the timing signal therefrom, wherein
the timing signal defines the predetermined exposure period.

2. The solid-state imaging apparatus of claim 1,
wherein the predetermined range is defined by upper and
lower limits, the first exposure information includes a

first exposure period, and the first exposure information generating circuit compares the level of the image signal with the upper and lower limits, decreases the first exposure period by a predetermined unit when the level of the image signal exceeds the upper limit and increases the first exposure period by the predetermined unit when the level of the image signal is below the lower limit.

3. The solid-state imaging apparatus of claim 2, wherein the second exposure information generating circuit receives exposure information selected from the selection circuit and calculates the second exposure information using a ratio of the selected exposure information to the level of the image signal and a reference value which corresponds to a reference exposure state.

4. The solid-state imaging apparatus of claim 1, wherein the first exposure information generating circuit further includes:

an exposure decision circuit for determining, every predetermined period, whether the level of the image signal output from the image sensor is within the predetermined range and generating a decision signal; and

an up/down counter, connected to the exposure decision circuit, for performing an up count operation or a down count operation in accordance with the decision signal, and generating the first exposure information.

5. The solid-state imaging apparatus of claim 4, wherein the second exposure information generating circuit includes a timing calculation circuit for receiving the exposure information selected by the selection circuit and calculating the second information which specifies an optimum exposure time using the selected exposure

information and the image signal.

6. The solid-state imaging apparatus of claim 1,
wherein the driver supplies a drain clock signal for
draining the information charges stored in the image sensor
and a transfer clock signal for transferring the stored
information charges, and the timing control circuit supplies
the driver with a second timing signal for producing the
drain clock signal and the transfer clock signal according
to the selected exposure information.

7. The solid-state imaging apparatus of claim 1,
wherein the image sensor generates an image signal for one
field during a vertical scan period and a plurality of
horizontal scan periods, and the first exposure information
generating circuit updates the first exposure information
every vertical scan period.

8. The solid-state imaging apparatus of claim 7,
wherein the second exposure information includes optimum
exposure time information.

9. A method for controlling an exposure period of a
solid-state imaging apparatus including a solid-state image
sensor which accumulates information charges corresponding
to an object image and generates an image signal in response
to the information charges, comprising the steps of:

driving the solid-state image sensor in accordance with
a timing signal so that the information charges are
accumulated within the exposure period and the image signal
is output;

determining whether a level of the image signal output
from the solid-state image sensor is within a predetermined
range and generating first exposure information based on the

determination results;

calculating second exposure information using the image signal output from the solid-state image sensor;

5 selecting the first exposure information when the level of the image signal is outside of the predetermined range and selecting the second exposure information when the level of the image signal is within the predetermined range; and

generating the timing signal for setting the exposure period in accordance with the selected exposure information.

10 10. The method of claim 9, wherein the solid-state image sensor generates the image signal for one screen during a vertical scan period and a plurality of horizontal scan periods, and the step of generating the first exposure information includes updating the first exposure information
15 every vertical scan period.

11. The method of claim 10, wherein the second exposure information includes optimum exposure time information.

ABSTRACT OF THE INVENTION

An imaging apparatus having a solid-state image sensor, such as a CCD, accumulates information charges corresponding to an image of an object and generates an image signal using the stored charges. A driver provides clock signals to the sensor which define vertical and horizontal scan periods, so that the information charges are accumulated in a predetermined exposure period, in accordance with a timing signal. A first exposure information generating circuit determines whether a level of the image signal is within an appropriate range and produces first exposure information based on the determination results. A second exposure information generating circuit calculates second exposure information using the image signal. A selector selects the first exposure information when the level of the image signal is outside of the predetermined exposure period and selects the second exposure information when the image signal is within the predetermined exposure period. A timing control circuit receives the selected exposure information from the selector and generates the timing signal.

Fig.1 (Prior Art)

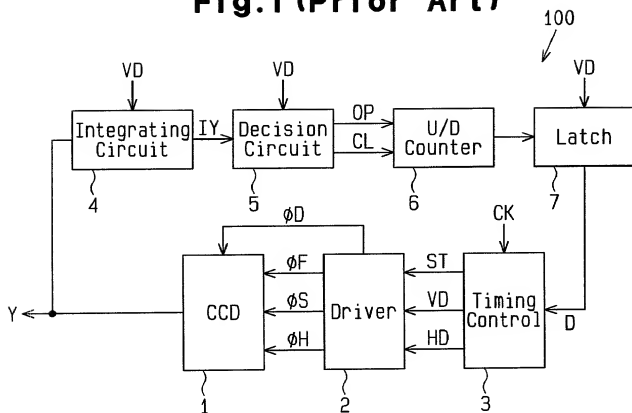


Fig.2 (Prior Art)

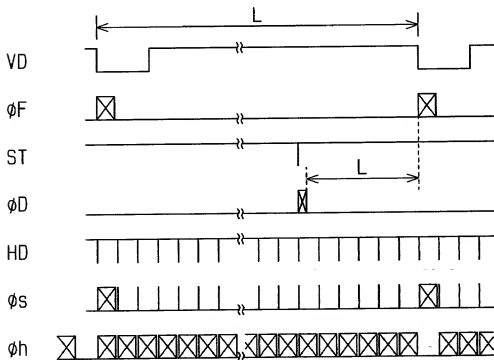


Fig.3

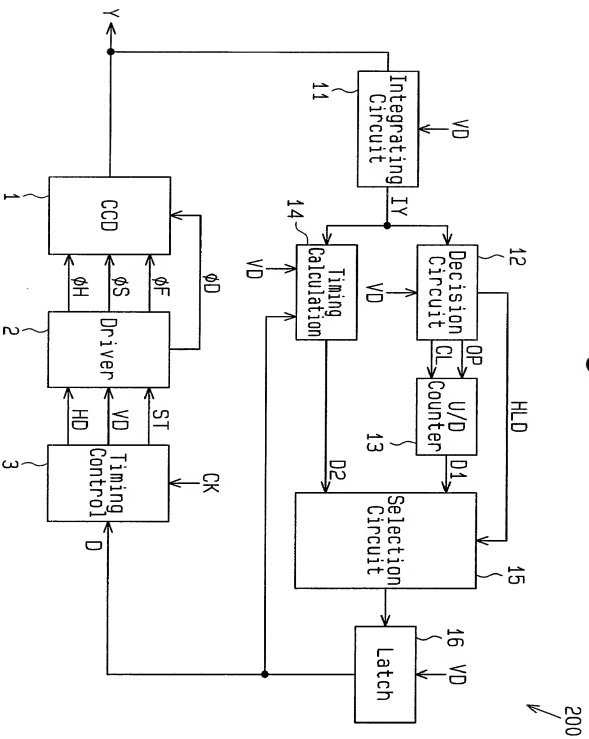
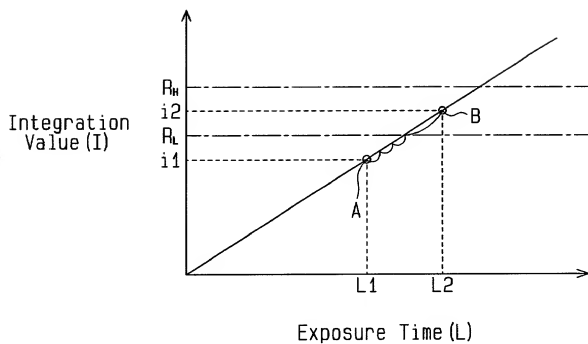


Fig.4



Declaration and Power of Attorney For Patent Application

特許出願宣言書

Japanese Language Declaration

私は、下欄に氏名を記載した発明者として、以下のとおり宣言する：

私の住所、郵便の宛先および国籍は、下欄に氏名に続いて記載したとおりであり、

名称の発明に関し、請求の範囲に記載した特許を求める主題の本来の、最初にして唯一の発明者である（一人の氏名のみが下欄に記載されている場合）か、もしくは本来の、最初にして共同の発明者である（複数の氏名が下欄に記載されている場合）と信じ、

その明細書を
(該当する方に印を付す)

☐ ここに添付する。

☐ _____ 日に出願番号

第 _____ 号として提出し、

_____ 日に補正した。

(該当する場合)

私は、前記のとおり補正した請求の範囲を含む前記明細書の内容を検討し、理解したことを陳述する。

私は、連邦規則法典第37部第1章第56条(a)項に従い、本願の審査に所要の情報を開示すべき義務を有することを認める。

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SOLID-STATE IMAGING APPARATUS WITH EXPOSURE

CONTROL

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as

Application Serial No. _____

and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Japanese Language Declaration

私は、合衆国法典第35部第119条にもとづく下記の外国特許出願または発明者証出願の外国優先権利益を主張し、さらに優先権の主張に係わる基礎出願の出願日前の出願日を有する外国特許出願または発明者証出願を以下に明記する:

Prior foreign applications
先の外国出願

Pat. Appln. No. 11-030377 (Number) (番号)	Japan (Country) (国名)	08 / 02 / 1999 (Day/Month/Year Filed) (出願の年月日)
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願の年月日)
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願の年月日)

Priority claimed
優先権の主張

<input checked="" type="checkbox"/> Yes あり	<input type="checkbox"/> No なし
<input type="checkbox"/> Yes あり	<input type="checkbox"/> No なし
<input type="checkbox"/> Yes あり	<input type="checkbox"/> No なし

私は、合衆国法典第35部第120条にもとづく下記の合衆国特許出願の利益を主張し、本願の請求の範囲各項に記載の主題が合衆国法典第35部第112条第1項に規定の態様で先の合衆国出願に開示されていない限度において、先の出願の出願日と本願の国内出願日またはPCT国際出願日の間に公表された連邦規則法典第37部第1章第56条(a)項に記載の所要の情報を開示すべき義務を有することを認める:

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) (出願番号)	(Filing Date) (出願日)
(Application Serial No.) (出願番号)	(Filing Date) (出願日)

(現況) (特許済み、係属中、放棄済み)	(Status) (patented, pending, abandoned)
(現況) (特許済み、係属中、放棄済み)	(Status) (patented, pending, abandoned)

私は、ここに自己の知識にもとづいて行った陳述がすべて真実であり、自己の有する情報および信ずるところに従って行った陳述が真実であると信じ、さらに故意に虚偽の陳述等を行った場合、合衆国法典第18部第1001条により、罰金もしくは禁錮に処せられるか、またはこれらの刑が併科され、またかかる故意による虚偽の陳述が本願ないし本願に対して付与される特許の有効性を損うことがあることを認識して、以上の陳述を行ったことを宣言する。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration

委任状: 私は、下記発明者として、以下の代理人をここに選任し、本願の手続を遂行すること並びにこれに関する一切の行為を特許商標庁に対して行うことを委任する。

(代理人氏名および登録番号を明記のこと)

David F. Zinger, Registration No. 29,127; Craig C. Groseth, Registration No. 31,713; Michael L. Tompkins, Registration No. 30,980; Todd P. Blakely, Registration No. 31,328; Gary J. Connell, Registration No. 32,020; Wannell M. Crook, Registration No. 31,071; Sabrina Crowley Stavish, Registration No. 33,374; Lewis D. Hansen, Registration No. 35,536; Joseph E. Kovarik, Registration No. 33,005; Douglas W. Swartz, Registration No. 37,739; John C. Scott, Registration No. 38,613; Bruce A. Kugler, Registration No. 38,942; Robert R. Brunelli, Registration No. 39,617; Chester E. Martine, Jr., Registration No. 19,711; Richard L. Hughes, Registration No. 31,264; Tejpal S. Hansra, Registration No. 38,172; Dana L. Hartje, Registration No. 40,638; Don D. Cha, Registration No. 40,945, of SHERIDAN ROSS P.C., 1700 Lincoln Street, Suite 3500, Denver, Colorado 80203.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

書類の送付先:

Send Correspondence to:

SHERIDAN ROSS P.C.
1560 Broadway
Suite 1200, Denver
Colorado 80202-5141

直通電話連絡先: (名称および電話番号)

Direct Telephone Calls to: (name and telephone number)

(303) 863-9700

唯一のまたは第一の発明者の氏名	Full name of sole or first inventor Toshio NAKAKUKI
同発明者の署名 日付	Inventor's signature Date <i>Toshio Nakakuki</i> February 2, 2000
住所	Residence Gifu-ken, Japan
国籍	Citizenship Japan
郵便の宛先	Post Office Address 1069-5, Honden, Hozumi-cho, Motosu-gun, Gifu-ken 501-0236 Japan
第2の共同発明者の氏名 (該当する場合)	Full name of second joint inventor, if any Tomomichi NAKAI
同第2発明者の署名 日付	Second Inventor's signature Date <i>Tomomichi Nakai</i> February 2, 2000
住所	Residence Ogaki-shi, Japan
国籍	Citizenship Japan
郵便の宛先	Post Office Address 2-18, Sanbongi, Ogaki-shi, Gifu-ken 503-0813 Japan

(第六またはそれ以降の共同発明者に対しても同様な情報および署名を提供すること。)

(Supply similar information and signature for third and subsequent joint inventors.)